The Future of Silicon-on-Insulator (SOI) Technology in Microelectronic Systems

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Abstract

After many years of materials development and circuit research, silicon-on-insulator (SOI) technology clearly has become a viable approach for high performance microelectronics. As semiconductor technology continues to scale, the value of an SOI materials platform continues to expand. It has become a key technology to enable a new class of micro-scale functionality, through 3-D circuits and mixed technology integration.

Introduction

Over the past decade, silicon-on-insulator (SOI) material has become the leading semiconductor platform for high performance devices and integrated circuits. The 2003 International Technology Roadmap for Semiconductors (ITRS) states that "near term measures such as the use of strained silicon channels are expected to provide needed boosts to device speed, but ultimately… [continued improvement] will require the replacement of bulk silicon substrates with silicon-on-insulator (SOI) substrates." [1] Apart from this inevitable shift, SOI offers a unique material system that will enable new modes of 3-D and heterogeneous integration.

SOI History

DARPA was initially interested in SOI device technology because of the lower supply voltage and sub-threshold leakage current as compared with bulk CMOS. This was viewed as providing a viable path to significant power reductions in high integration circuits. From the early days of SOI technology, DARPA and the Department of Defense had recognized the potential of SOI/SOS and actively fostered its development [2–4]. While thick-film SOI/SOS was initially investigated for application to space applications because of its radiation tolerance, the high performance and low power potential of thin-film SOI was also recognized. In the mid 1990's, DARPA initiated a major program to advance the state of art in SOI wafer technology and unambiguously demonstrated the technology with leading-edge devices and integrated circuits. This program extended research in the three viable technologies of that time; SIMOX [5], wafer bonding [6], and SOS [7]. As a result, major advances in materials quality were achieved and many of the key technical barriers to manufacturability were lowered.

The first challenge was to improve SOI material quality and reduce wafer production costs. At the beginning of the DARPA Low Power Electronics Program, leading-edge 200mm SOI wafers had unacceptable densities of defects and inclusions in the buried oxide, and poor surface qualities and finishes. The presence of gross crystalline defects such as pipes and stacking faults and the densities of etch defects made the prospects of highly integrated circuits on SOI a questionable undertaking. Performance limiting defects needed to be significantly reduced [8].

In conjunction with SEMATECH, a comprehensive series of low and medium dose SIMOX process technology experiments were sponsored by DARPA and a new oxygen implanter was developed to reduce implant time [5]. Experiments on post implantation anneals were also conducted. These efforts focused on ULSI materials for fully and partially depleted applications and resulted in a complete understanding of the process window for wafer

production [9,10]. Variants of these processes have been commercialized by program participants and have resulted in commercial manufacturing offerings [11]. Representative cross-sections and micrographs from these early SOI wafer process experiments are shown in Figure 1.

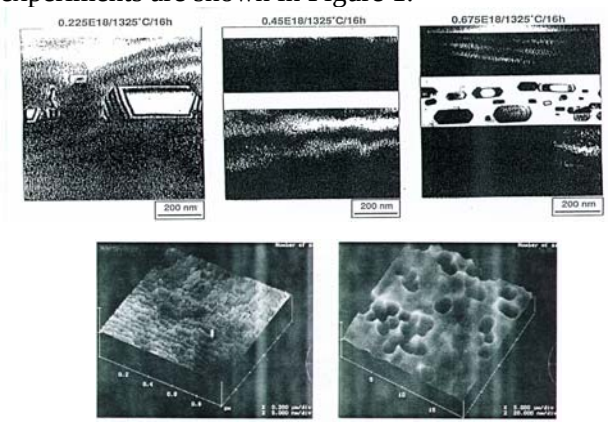

Figure 1. SOI material quality images from DARPA sponsored process experiments. Top row: cross-sections of SOI wafers with (left to right) incompletely formed buried oxide, complete and high quality buried oxide, and buried oxide with silicon island inclusions. Bottom row: Map of surface defects for a high quality (left) and lower quality (right) SOI wafer.

On the device side, DARPA's Advanced Microelectronics Program first demonstrated the feasibility of ultra large-scale integrated circuits fabricated on SOI, by demonstrating the process on a state-of-art (in the mid-1990's) 4 Mbit SRAM chip [12]. The performance and yield of this test chip convinced at least one company to focus its own resources on SOI as a high performance technology [11].

In the late 1990's, DARPA funded research to investigate very deeply scaled field-effect and tunneling transistors. The SOI substrate played a prominent role in the program, being the starting material of choice for nearly all of the participating research groups. Under the Advanced Microelectronics program, researchers developed a number of approaches to realize double-gate and gate-all-around structures, including the first reliably realizable double-gated transistor, the folded-channel FET [13]. This device evolved and became known as the finFET [14]. Figure 2 shows one of the first folded-channel FETs fabricated by researchers at the University of California at Berkeley. Other efforts in this program focused on variations of fully depleted device structures, referred to as slotFETs and Ultra Thin Body FETs [15].

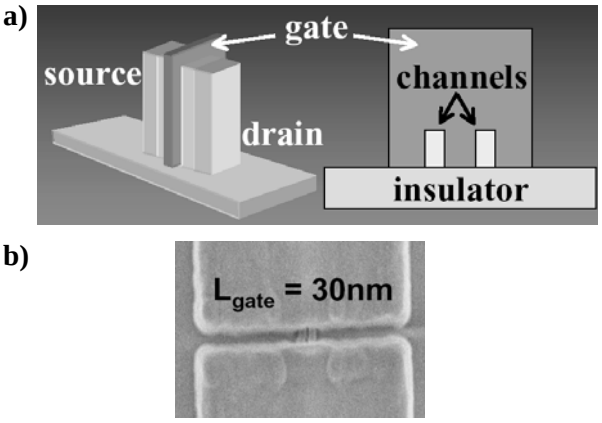

Figure 2. Folded-channel FET a) architecture diagram, and b) micrograph of device created under the Advanced Microelectronics program.

In the mid to late 1990's, several SOI substrate manufacturing approaches were fully commercialized, resulting in high quality, potentially low cost SOI by wafer bonding. These included deep ion implantation and anneal (SIMOX) [5], wafer bonding and etchback [6], and controlled etchback (SmartCut™) [7]. DARPA also sponsored research in advanced process and tools for ultra shallow junctions necessary for low power devices, including technologies like plasma immersion doping [16] and projection gas immersion laser doping (PGILD) to further extend this materials system and device concepts.

These techniques indeed resulted in excellent starting material and enabled DARPA to launch a significant effort to develop a more general approach to layer transfer and to create new classes of integrated microsystems using mixed materials and heterogeneous integration. Experiments were conducted which confirmed approaches to extract layers of compound semiconductors and transfer those layers to non-native substrates. Subsequent research was conducted to develop integrated fabrication processes or interconnection approaches. Nearly all of that work used silicon

and SOI as the integration platform and those results were encouraging [17].

The Next Opportunity: 3-D Integration

Using these results, DARPA is now exploring the use of SOI to realize a new class of novel device and integration concepts. SOI is particularly interesting as an approach to enable three-dimensional (3-D) microsystems. In a 3-D microsystem, the architecture is divided into a number of logical blocks, and each block is implemented on a separate semiconductor layer, or among a few layers. The layers are stacked vertically or horizontally and connected via interlayer interconnects. This allows for a much smaller chip footprint, and can alleviate clock synchronization issues by replacing long horizontal traces with much shorter interlayer connections. New design tools will be needed to make optimal use of these additional layers, and these are in development.

These 3-D circuits use the third dimension for more than additional wiring levels. A SOI based process may have advantages in simplifying the layer creation, separation, and transfer. Each layer of a 3-D IC contains active devices and layers are connected by a relatively high density of vertical vias in area arrays. These short vertical interconnections should have low parasitics and support very high bandwidths, providing a new fabric for on-chip communications, perhaps opening up new circuit architectures that may change the way data and signal processing is performed. It might also be the enabling hardware technology for cognitive and probabilistic computing [18]. Current wire limited designs such as field programmable gate arrays will benefit from 3-D processes [19]. In a general sense, 3-D integration will change the figure of merit for component integration from one of areal density to one of volumetric density.

DARPA is actively pursuing 3-D integration by investigating wafer-scale, chip-scale, and true 3-D processes, and by developing a new class of design tools and architectural exploration aids. The first experiments are focused on evaluating the yield and electrical performance of the vertical interconnects. Early work in the design area is focused on coupled electro-thermal modeling in support of optimizing floor planning and place/route of circuit blocks.

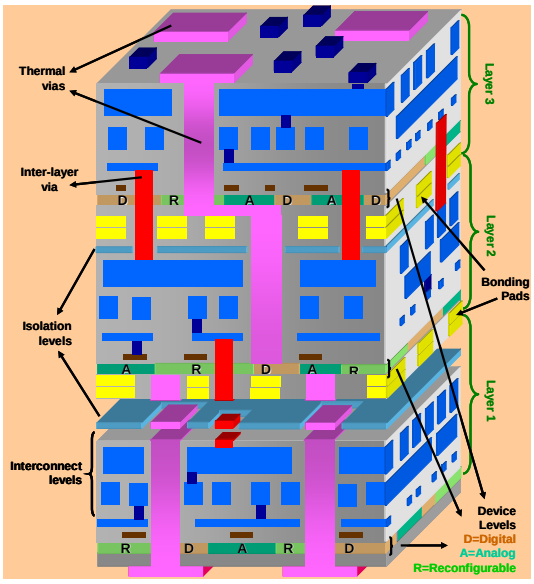

Figure 3. Schematic diagram of a prototypical 3-D integrated circuit with a high density of vertical interconnects between layers and carefully placed thermal vias.

Mixed Technology Integration

Another interesting opportunity in a 3-D integrated circuit comes from its ability to integrate heterogeneous materials and devices in different layers. In principle, layers can have different voltages, they can use synchronous or asynchronous logic, and they can be made of different materials. These might include compound semiconductors for low noise or very high speed, MEMS passive elements, such as high Q resonators, capacitors, and inductors, resulting in an entire high performance system-in-3-D chip with diminished need for off-chip elements. These 3-D microsystems could include analog and digital components, and they might include both electronic and photonic components on the same chip. Thus, 3-D integration is a functionally powerful technology that can be used to fabricate very high performance mixed-signal systems, and, again, SOI presents a logical platform for these microsystems.

An early demonstrator of this integration approach, DARPA launched the the Vertically-Integrated Sensor Arrays (VISA) program to constructing a multispectral imaging array using 3-D integration of heterogeneous circuits. As shown in Figure 4a, a typical CCD sensor system includes imaging pixels connected laterally with A/D converters, digital signal processors, image processors, and output ICs by chip-to-chip interconnects [21]. This results in a large device with a relatively small active area. The sampling rate and resolution are significantly limited by this interconnect approach. In the VISA approach, shown in Figure 4b, each of the subsystem components of the traditional design is replaced by layers of a 3-D IC. This results in devices that are much smaller, with more effective area and higher readout rates than are available today. The feasibility of the VISA approach has been demonstrated, and chips have been built which have demonstrated first images. Refinements are currently under way to improve operability and yield.

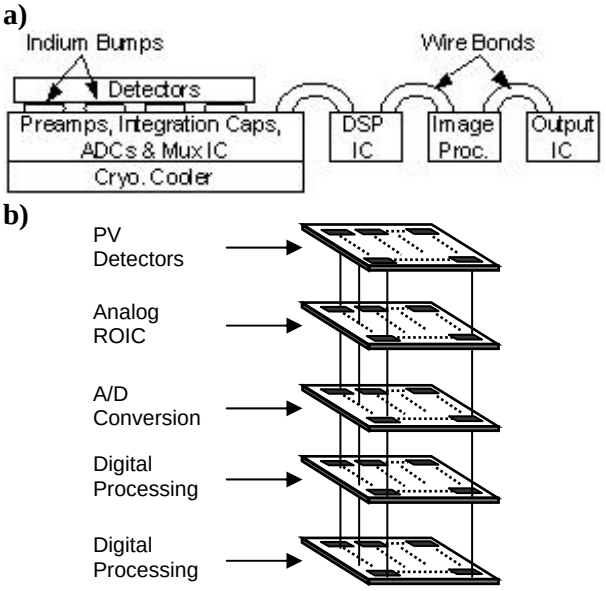

Figure 4. a) Traditional CCD sensor layout, b) VISA 3-D sensor layout.

Conclusion

With solid support from DARPA, the technical community has developed and inserted SOI as a leading platform for modern high performance microelectronics. The SOI materials system has become a key technology to enable a new class of micro-scale functionality, through 3-D circuits and mixed technology integration. The result of this work is beginning to demonstrate three dimensional functional scaling and has begun to open a new class of 3-D microsystems.

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References

[1] The International Technology Roadmap for Semiconductors (ITRS), 2003 Edition.

[2] Pakuti, L.J., et al., *Radiation Response of CMOS/SOI Devices Formed by Wafer Bond and Etchback*, IEEE Transactions on Nuclear Science, Vol. 35, Issue 6, Dec. 1998, pp. 1653-1656.

[3] Cohn, L., private communication.

[4] Lagnado, I., private communication.

[5] Blake, J. *SIMOX (Separation by Implantation of Oxygen)*, in Encyclopedia of Physical Science and Technology, 3rd ed., Vol. 14, Academic Press, 2002.

[6] Pitner, P. et al, *Wafer Bonded SOI Processes and Manufacturing Challenges*, Material Research Society spring 1996 meeting, Warrendale, PA.

[7] Celler, G. and Wolf, M., *Smart Cut™: A Guide to the Technology, the Process, the Products*, white paper available on SOITEC web site (unpublished).

[8] Colinge, J.-P., Silicon-on-Insulator Technology: Materials to VLSI, 3rd ed., Boston: Kluwer, 2004.

[9] DARPA Low Power Electronics Program Review, Reston, VA, April, 1995.

[10] SEMATECH S-90 Silicon-on-Insulator Project Report.

[11] Plouchart, J.O., et al., *Application of an SOI 0.12µm CMOS Technology to SoCs with Low*

Power and High Frequency Circuits, IBM J. Res., Vol. 47, No. 5/6, Sep./Nov. 2003, p. 611.

[12] DARPA Advanced Microelectronics Program Review, Reston, VA, 1997.

[13] Hisamoto, D., et al., *A Folded-Channel MOSFET for Deep-Sub-Tenth Micron Era*, IEDM Tech. Dig., Dec. 1998, pp. 1032-1034.

[14] Huang, X., et al., *Sub 50-nm FinFET: PMOS*, IEDM Tech. Dig., Dec. 1999, pp. 67-70.

[15] Chen, C.K., et al. *SLOTFET Fabrication of Self-Aligned Sub-100-nm Fully-Depleted SOI CMOS*, IEEE SOI Conference, Oct. 2000, p. 82.

[16] Qin, S., and Chan, C., *Plasma Doping for Semiconductor Experiments and Modeling*, Proceedings of DARPA Low Power Electronics Review Meeting, Reston, VA, May 13-15, 1996, pp. 301-318.

[17] Tong, Q.Y. *Wafer Bonding and Layer Splitting for Microsystems: An Overview*, 1999 International Meeting of the Electrochemical Society, Honolulu, HI.

[18] Bains, S., *Chip Stack Aims for Brain-Like Connectivity*, EE Times, October 13, 1998.

[19] Saraswat, K.C., et al., *Novel 3-D Structures*, IEEE Int. SOI Conf. Proceedings, pp. 54–55, 1999.

[20] Rieh, J.S., et al. *SiGe HBT with Cutoff Frequency of 350 GHz*, 2002 IEEE International Electron Devices Meeting (IEDM 2002), San Francisco, CA, 2002, p. 771.

[21] Schaper, L., *Vertically Interconnected Sensor Arrays (VISA)*, presented at the Pan Pacific Conference of the Surface Mount Technology Association (SMTA), Kahuku, HI, February 12, 2004.